REMARKS/ARGUMENTS

The Examiner is thanked for the thorough examination and search of the subject patent application.

Claims 25, 28, 29, 31-35 and 45-48 are pending. Claims 25, 28, 29, 31-35 and 45 are currently amended. Claims 46-48 are newly added. Claims 1-24, 26, 27, 30 and 36-44 are canceled.

Response to Claim Rejections under 35 U.S.C. 102

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 25, 28, 29, 31-35, and 45

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As currently amended, independent claim 25 is recited below:

25. A chip package comprising:
a first semiconductor chip;
a second semiconductor chip joined with a top surface of said first semiconductor chip;
a first insulating layer covering a sidewall of said second semiconductor chip and said top surface of said first semiconductor chip, wherein said first insulating layer comprises a top surface substantially parallel to said top surface of said first semiconductor chip; and
a metal layer over said top surface of said first insulating layer.

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Reconsideration of the rejections under 35 U.S.C. 102(b) to Claims 25-29, 31-35 and 45 as being anticipated by Tokuda et al. (US5,870,289) is respectfully requested based on the following remarks.

Applicants respectfully assert that the circuitry component claimed in claim 25 patentably distinguishes over the citation by Tokuda et al. (US5,870,289).

Tokuda et al. teach a chip package comprising a wiring substrate 220-n, a chip 210-n joined with a top surface of said wiring substrate 220-n, an insulating layer 260-n covering a sidewall of said chip 210-n and said top surface of said wiring substrate 220-n, wherein said insulating layer 260-n comprises a top surface substantially parallel to said top surface of said wiring substrate 220-n. The chip package further comprises a metal layer 281 over said top surface of said insulating layer 260-n. ~ *See Fig. 4* ~

Tokuda et al. teach a chip 210-n joined with a top surface of a wiring substrate 220-n (col. 15, lines 53-54). It is believed that wiring substrate 220-n cannot to be deemed to be a semiconductor chip. Accordingly, Tokuda et al. fail to teach the chip 210-n can be joined with a top surface of a semiconductor chip, as claimed in Claim 25. Withdrawal of rejection under 35 U.S.C. 102(b) to Claim 25 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 25 patentably distinguishes over the prior art references, and should be allowed.

For at least the same reasons, dependent claims 28, 29, 31-35 and 45-48 patentably define over the prior art as well.

CONCLUSION

Some or all of the pending claims are now believed to be in condition for allowance. Accordingly, allowance of the claims and of the application as a whole is respectfully requested.

It is requested that should the Examiner not find that the Claims are now Allowable that the Examiner call the undersigned at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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